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H1K

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(54) Dielectrically-isolated integrated circuit manufacture

(57) An integrated circuit is manufactured with circuit elements formed in dielectrically-isolated semiconductor islands (1,2 etc) which are bounded at least at their bottom by insulating material (20). In the formation of these islands grooves (12) are etched into a major surface (13) of a monocrystalline semiconductor body (11) in such a pattern as to leave semiconductor mesas (14), then dielectrically-isolated islands are formd from an upper part (14') of the semiconductor mesas (14) and a lower part of each semiconductor mesa (14) is subjected via the grooves (12) to a chemical conversion treatment, e.g. oxidation of silicon which converts this lower part laterally over the whole of its width into the bottom insulating material (20) thereby isolating the upper part (14') of each mesa from an underlying portion of the semiconductor body (11). Before the chemical conversion treatment, the side-walls of the grooves (12) may be etched laterally beneath the upper part (14') of each semiconductor mesa, and the side walls of the upper part (14') of the semiconductor mesa (14) may even be masked during the conversion treatment for forming the bottom insulation (20) of the islands. An upper part of the dielectrically-isolated semiconductor islands may be formed by epitaxial growth on the semiconductor mesas.

Fig.2.

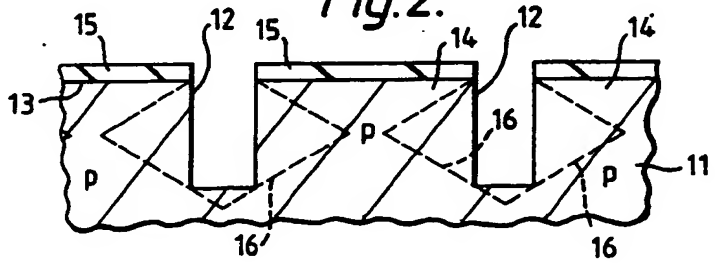

Fig.3.

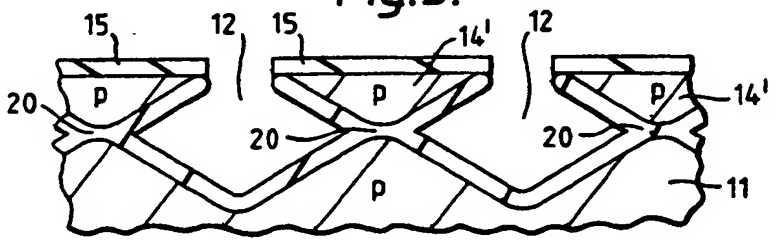

Fig.4.

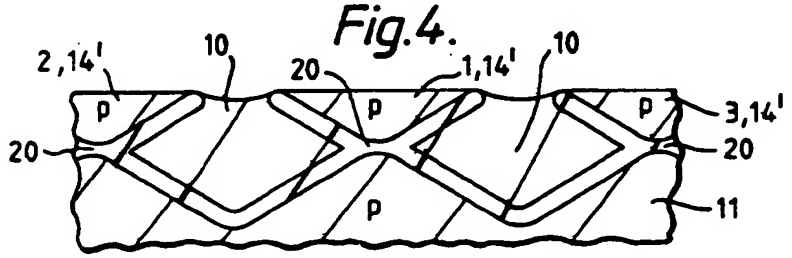

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Fig. 1.

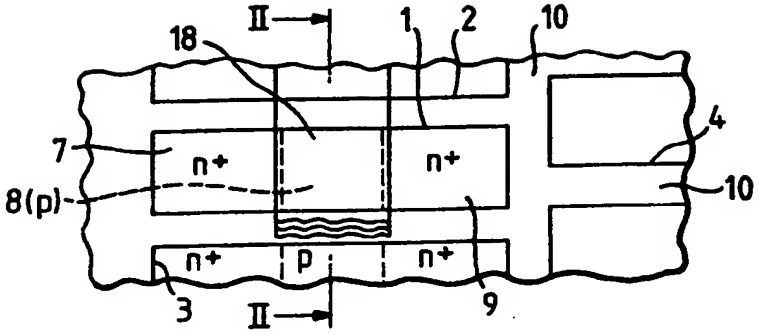


Fig. 2.

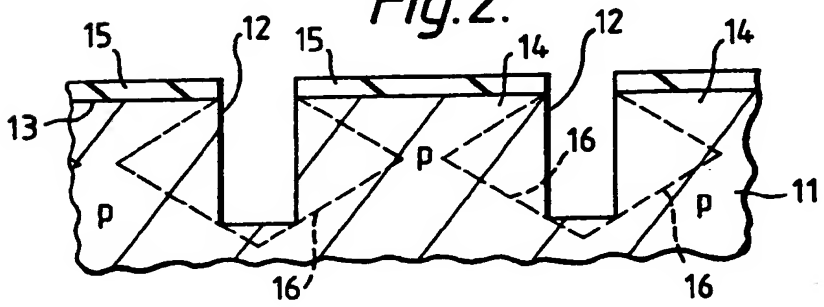


Fig. 3.

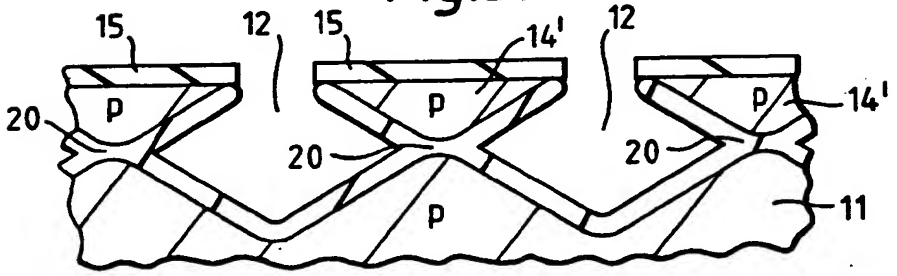


Fig. 4.

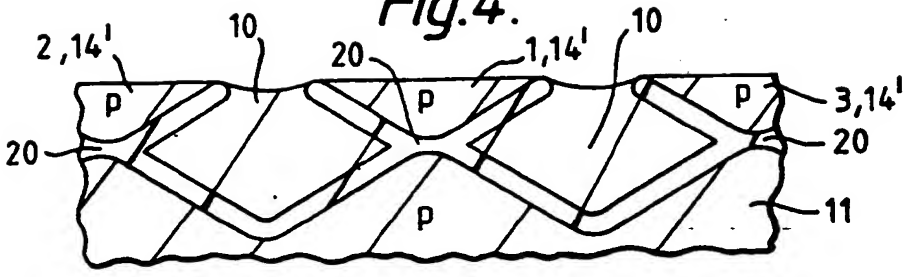


Fig.5.

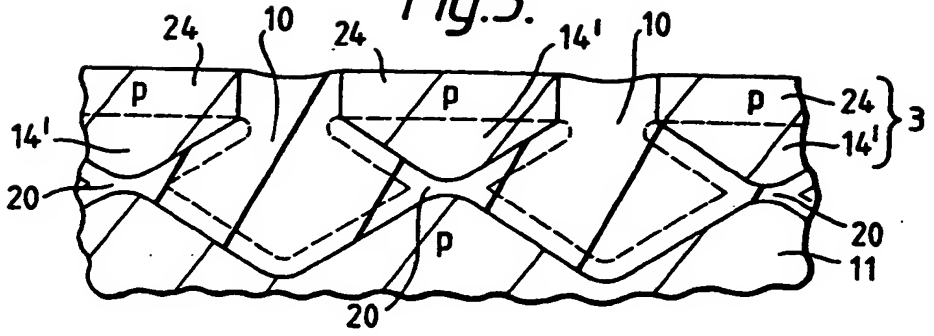


Fig.6.

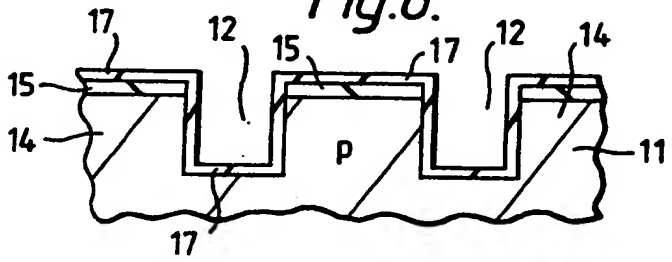


Fig.7.

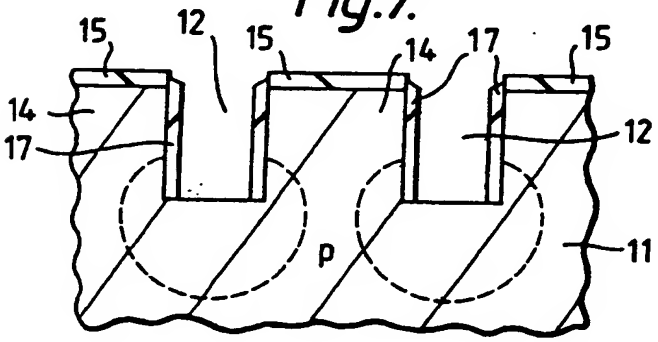
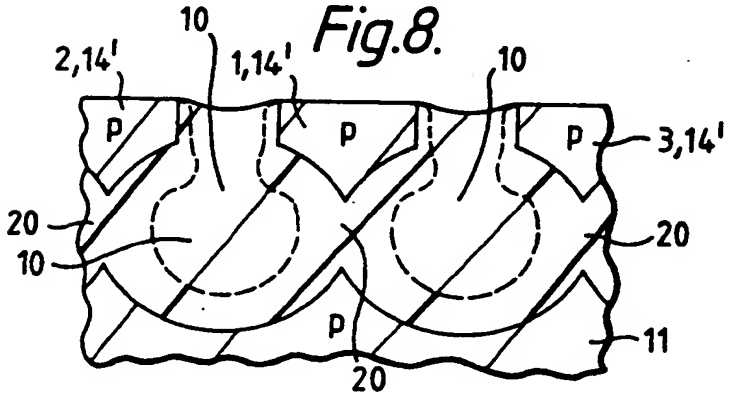


Fig.8.



SPECIFICATION

Integrated circuit manufacture

This invention relates to methods of manufacturing an integrated circuit comprising circuit elements formed in dielectrically-isolated semiconductor islands which are bounded at least at their bottom by insulating material, particularly but not exclusively silicon islands bounded by thermally grown silicon dioxide.

Dielectric isolation is becoming increasingly desirable in integrated circuits to improve radiation hardness, reduce parasitic capacitances and avoid parasitic device element structures. Since the 1960s a variety of technologies have been tried to achieve dielectric isolation, see for example the magazine 'Electronics' published by McGraw-Hill, Vol 40 No 6, March 20th 1967, pages 91 to 108 for a general survey.

In one form in which there is still considerable interest, the semiconductor islands are formed by depositing a layer of, for example, silicon on an insulating substrate of, for example sapphire. The deposition conditions are chosen so as to achieve as far as possible epitaxial growth of a single crystal semiconductor layer on the substrate. Grooves are subsequently etched into the upper major surface of the layer in such a pattern as to leave semiconductor mesas.

The grooves may be etched through the entire thickness of the layer so that the mesas from the islands which are dielectrically isolated at their bottom by the insulating substrate and which are dielectrically isolated laterally by the air in the grooves. One example of such a silicon-on-sapphire integrated circuit is illustrated on page 107 of said 'Electronics' magazine.

However, U.K. patent specification GB–A 1208576 describes an advantageous modification in which the grooves are etched through only part of the thickness of the silicon layer after which the remaining silicon at the grooves is converted by an oxidizing treatment into a silicon dioxide isolation pattern through the entire thickness of the layer. This chemical conversion is therefore used to isolate dielectrically the islands laterally from each other, and a substantially plane upper surface of both the silicon islands and the silicon dioxide pattern can be obtained. The islands remain dielectrically isolated at their bottom by the insulating substrate material, for example, sapphire.

However, the crystalline quality of silicon islands formed from a layer deposited on an insulating substrate tends to be poor due to the mismatch in the crystal lattices and possibly thermal expansion coefficients of the different materials for the substrate and the layer. Furthermore unwanted doping of the silicon islands by aluminium diffusion from a sapphire substrate can also degrade the semiconductor quality of the islands. The crystalline quality of the semiconductor islands can affect the characteristics and performance of the circuit elements formed in the islands, for example, by increasing leakage currents.

According to the present invention there is provided a method of manufacturing an intergrated circuit comprising circuit elements formed in dielectrically-isolated semiconductor islands which are bounded at least at their bottom by insulating material, wherein as a step in the formation of these islands grooves are etched into a major surface of a monocrystalline semiconductor body in such a pattern as to leave semiconductor mesas from which the islands are formed, characterized in that the dielectrically-isolated islands are formed from an upper part of the semiconductor mesas, a lower part of each semiconductor mesa being subjected via the grooves to a chemical conversion treatment which converts said lower part laterally over the whole of its width into said insulating material thereby isolating the upper part of each mesa from an underlying portion of the semiconductor body.

Such a method in accordance with the invention permits the obtaining of dielectrically-isolated semiconductor islands of good crystal quality from the semiconductor body by vertically isolating these parts from the underlying portion of the semiconductor body. It is particularly suitable for forming these islands with small dimensions such as are becoming increasingly desirable for very large scale integration of semiconductor circuits. The isolated upper parts of the mesas may be formed with sufficient dimensions to constitute the dielectrically-isolated islands in which the circuit elements are formed. However, since such good crystal quality can be obtained for these isolated upper parts, the upper parts of the mesas may be isolated by the conversion treatment and then thickened by epitaxial growth of semiconductor material to form an upper part of the dielectrically-isolated islands on the isolated upper parts of the mesas.

The complete pattern of grooves for defining the islands may be etched into the body in more than one stage. Thus, for example, if the islands to be formed are rectangular in plan view, grooves may first be etched for one pair of opposite sides of the rectangle which may then be subjected to the chemical conversion treatment to form the bottom insulating material between this pair of sides, after which grooves may be etched for the other pair of opposite sides of the rectangle to complete the lateral isolation of the islands. It is also possible to etch the grooves for a pair of opposite sides in different stages and to effect chemical conversion of a part of the body between these different etching stages to form part of the bottom isolation of the

islands. The chemical conversion to form the bottom isolation may be effected in more than one stage.

Various techniques may be used for chemically converting the lower part of the mesas into the insulating material while retaining a useful area of semiconductor material over at least a part of the width of the upper part of the mesas. A masking layer may be provided for example, on the side walls of at least the upper part of each semiconductor mesa to mask this upper part during the chemical conversion treatment, and/or the grooves may be formed with side-walls so shaped that the upper part is wider than the part which is to be converted.

Particularly when the insulating material occupies a larger voluem than that of the semiconductor material which was converted to form the insulating material (for example as occurs with silicon dioxide formed by oxidation of silicon) it is desirable, before the chemical conversion treatment, to etch the side-walls of the grooves laterally beneath the upper part of each semiconductor mesa so as to at least reduce the width of this lower part of the mesa and produce an overhanging upper part of the semiconductor mesa which may be supported on a lower part of reduced width.

The grooves may be formed using one etching treatment after which a different etching treatment may be used to reduce the width of the lower part of each semiconductor mesa. Thus use may be made of the different characteristics of different etching treatments (for example different etch rates perpendicular and parallel to the major surface), and for example narrow deep grooves may be etched to form closely-packed dielectrically-isolated islands so increasing the packing density of the integrated circuit.

These and some other features in accordance with the invention will now be illustrated more specifically, by way of example, in embodiments of the invention described with reference to the accompanying diagrammatic drawings. In these drawings:

Figure 1 is a plan view of part of an integrated circuit having dielectrically-isolated islands formed in accordance with the present invention;

Figure 2 is a cross-section on the line II–II of Fig. 1 at an early stage in its manufacture by a method in accordance with the present invention,

Figures 3 and 4 are similar cross-sectional views of the body part of Fig. 2 at subsequent stages in the manufacture according to one embodiment of the invention;

Figure 5 is a similar cross-sectional view of the body part of Fig. 4 showing a possible subsequent stage in manufacture, and

Figures 6 to 8 are cross-sectional views of a body part similar to that of Fig. 2 at subsequent stages in the manufacture according to another embodiment of the invention.

It should be noted that all the Figures are diagrammatic and not drawn to scale. The relative dimensions and proportions of parts of these Figures have been shown exaggerated or diminished for the sake of clarity and convenience in the drawings. The same reference numeral as used in one embodiment are generally used to refer to corresponding or similar parts in the other embodiments.

The integrated circuit illustrated in Fig. 1 comprises circuit elements formed in dielectrically-isolated semiconductor islands 1, 2, 3, 4 etc which are bounded at least at their bottom by insulating material 20 (see Figs. 4, 5 and 8). By way of example Fig. 1 illustrates in each of islands 1 and 3 two *n* type regions 7 and 9 which are formed by overdoping parts of the island 1, 3 and which are separated by the remaining *p* type part 8 of the island 1, 3. These regions 7, 8 and 9 may form the source, channel area, and drain respectively of a field-effect transistor having an insulated gate 18 overlying the channel area 8.

The islands 1, 2, 3, 4 etc may be dielectrically isolated laterally by air gaps in the form of a pattern of grooves which extend to the depth of the insulating material 20 at the bottom of the islands. This however, forms a non-planar upper surface and renders more difficult the provision of conductive layer connections between the circuit elements in different islands. Therefore it is preferable for the grooves to be filled with material 10 which is electrically insulating at least at the walls of the islands and which provides the integrated circuit with a substantially plane upper surface.

Most integrated circuits manufactured at present are of silicon, and so, for the purpose of detailed examples of the embodiments of the invention, the manufacture of a silicon integrated circuit will be described having monocrystalline silicon islands 1, 2, 3, 4 etc dielectrically-isolated at their bottom by silicon dioxide 20 and dielectrically-isolated at least at their walls by silicon dioxide or/and silicon nitride. However, it will be evident that the invention may be used with other insulating materials which can be formed by chemical conversion of the semiconductor material (for example, silicon nitride formed by nitriding silicon) and with other semiconductor materials (for example gallium arsenide which can be anodized to form an insulating oxide).

The starting material in the manufacture of an integrated circuit such as that of Fig. 1 is a monocrystalline semiconductor body 11 of for example silicon. The body 11 may consist of a uniformally doped wafer of for example *p* type silicon, or it may already contain differently doped regions. In one form it may consist of low-doped *p* type silicon epitaxial layer on a mono-crystalline highly-doped *p*

type silicon substrate.

As a step in the formation of the islands 1, 2, 3, 4 etc, grooves 12 are etched into a major surface 13 of the body 11 in such a pattern as to leave semiconductor mesas 14 from which the islands are subsequently formed. In order to obtain a high packing density these grooves 12 are preferably deep and narrow. They may be formed with substantially vertical side-walls using directional etching by means of, for example, a parallel-plate plasma system or an ion beam or reactive ion etching, while masking the top of the mesas 14 with a masking layer pattern. Such an etching treatment has a fast etch rate perpendicular to the surface 13 with very little lateral etching below the masking layer pattern 15 and parallel to the surface 13.

This masking layer pattern may comprise a photoresist layer on a layer 15 of, for example, silicon nitride. The silicon nitride layer 15 may be retained for use as a mask during subsequent processing steps. The resulting structure is illustrated in Fig. 2.

In the following steps of the embodiment as illustrated in Fig. 3 an etchant whose etching rate is dependent on the crystal lattice orientation of the body 11 is used to at least reduce the width of a part of each mesa 14 beneath an upper part from which the islands 1, 2, 3, 4 etc are subsequently formed. In this case, for example, the major surface 13 of the silicon body 11 may have been initially chosen to be a {110} oriented crystal plane, and the masking layer pattern may have been so orientated that the grooves 12 are formed with {100} oriented crystal planes as their side walls perpendicular to the surface 13. The width of a lower part of each mesa 14 beneath the upper part may now be reduced using an orientation-dependent etchank such as a hot solution of potassium hydroxide or a hot solution of pyrocatechol and ethylene diamine or hydrazine which has a slow etching rate on {111} oriented crystal planes. Therefore, this etchant etches the silicon side-walls of the mesas 14 until encountering {111} crystal planes, which are indicated by the broken lines 16 in the cross-sectional view of Fig. 2.

If the grooves are completely etched to {111} planes, the width of the masking layer 15 on the top of the mesa together with the depth of the original vertical grooves 12 determine both the remaining width of silicon between the {111} planes at the narrowest part of the mesa 14 as well as the depth of the upper part. In a particular specific example, the masking layer parts 15 may be 3.5×10^3nm (nanometres) wide and the vertical grooves may be etched to a depth of 2×10^3nm. If the grooves are then completely etched to {111} planes the remaining width of silicon between the {111} planes at the narrowest part of the mesa is 7×10^2 nm.

In the next step illustrated in Fig. 3 the side walls of the mesas 14 are subjected via the grooves to a chemical conversion treatment which converts the reduced-width part laterally over the whole of its width into insulating material 20. In the case of silicon mesas this conversion can be effected very conveniently by thermal oxidation using the silicon nitride layer 15 to mask the top of the mesas 14. The resulting structure as illustrated in Fig. 3 comprises the upper silicon parts 14′ of the mesas 14 isolated vertically from the bottom of the mesas 14 and from the underlying silicon body portion by the merging of the grown silicon dioxide 20 which also coats the side-walls of these upper parts of the mesas 14. The grooves 12 of the Fig. 3 structure may be unfilled with any further material in the final integrated circuit, in which case the circuit element regions 7, 9 etc may now be formed in the upper parts 14′ of the mesas, these upper parts 14′ constituting the dielectrically-isolated islands 1, 2, 3, 4 etc of the integrated circuit.

However, as illustrated in Fig 4 it is preferable to fill the grooves 11 with suitable material 10 to provide the integrated circuit with a substantially plane upper surface both of the islands 1, 2, 3, 4 etc and of the intermediate filler material 10. For this purpose silicon dioxide, polycrystalline silicon or other suitable material may be provided to fill the grooves 12. The infilling may be effected by deposition in several stages, using directional etching between the deposition stages to remove deposited material from exposed horizontal surfaces. Polycrystalline silicon may be used since the upper parts 14′ of the mesas are already dielectrically-isolated laterally by the silicon dioxide grown on their side-walls in the oxidation step of Fig. 3. An advantage of the use of silicon as a filler material 10 is that its thermal expansion coefficient more closely matches that of the monocrystalline silicon islands 1, 2, 3, 4 etc. The resulting structure of Fig. 4 may then be provided with the circuit element regions 7, 9 etc, the upper silicon parts 14′ of the mesas constituting the dielectrically-isolated islands 1, 2, 3, 4 etc of the integrated circuit.

However, Fig. 5 illustrates a further modification in which an upper part 24 of the dielectrically-isolated semiconductor islands 1, 2, 3, 4 etc is formed by selective epitaxial growth of silicon on the upper part 14′ of the mesas, after removing the masking layer pattern 15 from the structure of Fig. 3. Thicker silicon islands are obtained in this way, constituted by the parts 14′ and 24. Similar filler materials 10 may be deposited in the gaps between the islands to provide a plane upper surface for the integrated circuit.

It is also possible to form deeper but narrower upper parts 14′ of the mesas by using the same orientation dependant etchant solu-

tions to form {111} sided grooves with a silicon body 11 having a major surface 13 formed by a {100} plane and with the masking layer pattern 15 so orientated that the initially vertically-sided grooves 12 are formed with {110} side walls. A {100} major surface 13 is often preferred for surface-adjoining channels of MOS transistors.

In order to reduce the width of the lower part of the mesas 14 it is not necessary to use an etchant whose etching rate is dependant on the crystal lattice orientation. An example of an alternative method will now be described with reference to Figs. 6 and 8. In this example, after forming the grooves 12 with sidewalls substantially perpendicular to the surface 13 as in the Fig. 2 structure, a further masking layer 17 may be deposited to coat the whole upper surface of the Fig. 2 structure, i.e. the silicon nitride masking layer 15, and the side-walls and bottom of the grooves 12, as illustrated in Fig. 6. This masking layer 17 may also be of silicon nitride. A directional etching treatment such as plasma etching or ion beam milling is then used to remove this silicon nitride coating from the horizontal surfaces (of the silicon nitride layer 15 and the bottom of the grooves 12) but not from the vertical side-walls of the grooves 12.

Both the grooves 12 and the mesas 14 are now deepened using a different etching treatment, for example with an isotropic etchant solution such as a mixture of nitric, hydrofluoric and acetic acids. During this etchant treatment the upper part of each semiconductor mesa is masked by the masking layer 17 on its side-walls, while the etchant removes silicon both laterally and vertically at the exposed bottom of the grooves 12 to form a deeper mesa 14 having a masked wide upper part 14 supported on a narrowed lower part. The extent of this etching is illustrated by the broken line 18 in Fig. 7.

While using the silicon nitride layers 15 and 17 as an oxidation mask on the wide upper part 14 of these mesas, the semiconductor structure is then subjected to a thermal oxidation treatment to grow silicon dioxide 20 laterally across the whole width of the bottom of these upper parts 14 of the mesa. Depending on the thickness and density of the nitride layer 17 on the side-walls, this layer 17 may be converted partly or even wholly into silicon dioxide in this oxidation treatment. The insulating layer 17 of silicon nitride or/and silicon dioxide may be retained for lateral isolation purposes in the final integrated circuit structure, and the grooves 12 may be filled with deposited silicon dioxide, polycrystalline silicon or other suitable material 10. The remaining upper silicon parts 14 form the islands 1, 2, 3, 4 etc which are dielectrically-isolated vertically from the underlying portion of the silicon body 11 by the insulating material 20. The circuit element regions 7, 9 etc are formed in these islands.

Compared with the lattice-orientation dependant process of Figs. 3 and 4, the embodiment of Figs. 6 to 8 facilitates the obtaining of wide deep islands 1, 2, 3, 4 since the reduction in the width of part of the mesa resulting from the lateral etching does not start at the upper surface 13 but at the bottom of the grooves 12. Furthermore, the process of Figs. 6 to 8 provides greater freedom of choice in orientation of the silicon body faces. Thus, for example the silicon dioxide coating on {111} silicon faces at the side-walls of the silicon islands of Figs. 3 and 4 may have a quite high electronic charge which may be undesirable in some integrated circuits such as for example *n* channel MOSICs.

It will be evident that many other modifications are possible within the scope of the invention. Thus, for example when the starting body 11 comprises a low-doped *p* type silicon epitaxial layer on a monocrystalline highly-doped *p* type silicon substrate, the highly-doped substrate which has a lower etching rate can function to restrict downward etching of the grooves at least during an etching treatment which is used to form a reduced width part of the mesas 14 below overhanging upper mesa parts.

The provision of silicon nitride directly on monocrystalline silicon can sometimes strain the silicon crystal lattice. Thus the silicon nitride layer or layers 15 (and 17) may be provided on a thin layer of, for example, thermally-grown silicon dioxide, and a silicon dioxide layer may also be deposited at least on the nitride layer 15.

Although generally desirable to mask the top surface of the mesas 14 against oxidation so as to retain a maximum thickness for the remaining upper silicon part after oxidation, the silicon nitride layer 15 may be replaced by a silicon dioxide layer or a photoresist layer both of which will provide an etchant mask for forming the grooves 12, at least the photoresist layer being removed before the oxidation treatment. Although these materials are most commonly used in the manufacture of silicon integrated circuits, it will be evident that other materials are also suitable.

If all the grooves 12 are etched simultaneously to form a pattern corresponding to the complete lateral isolation pattern of the islands, it will be evident that the lateral etching to reduce the width of a lower part of the mesas 14 must be terminated before etching across the whole width of the mesas. However, two separate stages may be used to form the complete pattern of grooves 12 and dielectric-isolation of the upper parts of the mesas 14. Thus for example the grooves 12 which extend in one direction across the surface 13 of the semiconductor body 11 (e.g. in

the direction along the longitudinal sides of the islands 1, 2 and 3 in Fig. 1) may be etched first and the dielectric-isolation 20 may then be formed across the bottom of the mesas 14 between these first grooves 12, after which the pattern may be completed by etching second grooves 12 (e.g. in the direction of the shorter end sides of the islands 1, 2, and 3 in Fig. 1) to complete the dielectric-isolation. In this case the lateral etching between the upper part of the mesas 14 defined by the first grooves may be continued to completely remove the semiconductor material beneath these upper parts and the underlying body portion since these upper parts remain attach to the body 11 at, for example, their shorter end sides. This facilitates accommodation of the insulating material 20 in the semiconductor body 11 particularly when the insulating material 20 formed by chemical conversion of the semiconductor material occupies a larger volume than the converted semiconductor material.

It is also possible to etch grooves 12 and provide buried dielectric isolation 20 first from one longitudinal side of each island and then to effect the process at the opposite longitudinal side. Furthermore, in some methods in accordance with the invention it is not necessary to reduce the width of a lower part of the mesas 14 before the chemical conversion treatment, especially if the side walls of the upper part of the mesas are masked against the conversion treatment. The bottoms of the grooves 12 may even be subjected to a different (non-etchant) treatment such as for example an electrolytic treatment to facilitate chemical conversion of a lower part of the mesas 14 into insulating material 20 while retaining semiconductor material in an upper part of the mesas 14.

CLAIMS

1. A method of manufacturing an integrated circuit comprising circuit elements formed in dielectrically-isolated semiconductor islands which are bounded at least at their bottom by insulating material, wherein as a step in the formation of these islands grooves are etched into a major surface of a monocrystalline semiconductor body in such a pattern as to leave semiconductor mesas from which the islands are formed, characterized in that the dielectrically-isolated islands are formed from an upper part of the semiconductor mesas, a lower part of each semiconductor mesa being subjected via the grooves to a chemical conversion treatment which converts said lower part laterally over the whole of its width into said insulating material thereby isolating the upper part of each mesa from an underlying portion of the semiconductor body.

2. A method as claimed in Claim 1, further characterized in that, before the chemical conversion treatment, the side-walls of the grooves are etched laterally beneath the upper part of each semiconductor mesa to reduce the width of the lower part of the mesa and produce an overhanging upper part of the semiconductor mesa supported on the lower part of reduced width.

3. A method as claimed in Claim 2, further characterized in that the grooves are formed in the major surface using one etchant treatment after which a different etching treatment is used to reduce the width of the lower part of each semiconductor mesa.

4. A method as claimed in Claim 3, further characterized in that the grooves are first formed with side-walls substantially perpendicular to said major surface using a directional etching treatment which etches the semiconductor material of the body faster in a direction perpendicular to said major surface than in a direction parallel to said major surface.

5. A method as claimed in Claim 3 or Claim 4, further characterized in that said major surface is a {110} orientated crystal plane of a monocrystalline silicon semiconductor body, and the grooves are first formed with {100} orientated crystal planes as their side-walls perpendicular to said major surface, after which an etchant which has a slow etching rate on {111} orientated crystal planes is used to reduce the width of the lower part of each semiconductor mesa.

6. A method as claimed in any one of Claims 2 to 5, further characterized in that a masking layer is provided on the side-walls of at least the upper part of each semiconductor mesa to mask this upper part during the etching treatment for producing a lower part of reduced width.

7. A method as claimed in any one of the preceding Claims further characterized in that a masking layer is provided on the side-walls of at least the upper part of each semiconductor mesa to mask this upper part during the chemical conversion treatment for converting the lower part into said insulating material.

8. A method as claimed in Claim 7 when appendant to Claim 6, further characterized in that at least part of the masking layer for the etching treatment is retained as at least part of the masking layer for the chemical conversion treatment.

9. A method as claimed in any one of the preceding Claims, further characterized in that an upper part of the dielectrically-isolated semiconductor islands is formed by epitaxial growth of semiconductor material on the upper part of the semiconductor mesas.

10. A method as claimed in any one of the preceding Claims, further characterized in that, after the chemical conversion treatment, filler material is provided at the area of the grooves to provide the integrated circuit with a substantially plane upper surface both of the islands and of the intermediate filler material.

11. A method as claimed in any one of

the preceding Claims, further characterized in that at least the part of the semiconductor body from which the mesas are formed is of silicon, and in that the chemical conversion treatment is performed by oxidation of the lower part of each silicon mesa.

12. A method of manufacturing an integrated circuit substantially as described with reference to Figs. 2 to 4 or Fig. 5 of Figs. 6 to 8 of the accompanying drawings.

13. An integrated circuit manufactured by a method claimed in any one of the preceding claims.

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